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### 1 [Cache inclusion and processor sampling in multiprocessor simulations](#)



Jacqueline Chame, Michel Dubois

 June 1993 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1993 ACM SIGMETRICS conference on Measurement and modeling of computer systems SIGMETRICS '93**, Volume 21 Issue 1

Publisher: ACM Press

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The evaluation of cache-based systems demands careful simulations of entire benchmarks. Simulation efficiency is essential to realistic evaluations. For systems with large caches and large number of processors, simulation is often too slow to be practical. In particular, the optimized design of a cache for a multiprocessor is very complex with current techniques. This paper addresses these problems. First we introduce necessary and sufficient conditions for cache inclusion in systems with invalid ...

### 2 [Execution-driven simulation of multiprocessors: address and timing analysis](#)



S. Dwarkadas, J. R. Jump, J. B. Sinclair

 October 1994 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 4 Issue 4

Publisher: ACM Press

 Full text available: [pdf\(1.58 MB\)](#)

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This article describes and evaluates an efficient execution-driven technique for the simulation of multiprocessors that includes the simulation of system memory and that is driven by real program work loads. The technique produces correctly interleaved address traces at run-time without disk access overhead or hardware support, allowing accurate simulation of the effects of a variety of architectural alternatives on programs. We have implemented a simulator based on this technique that offe ...

**Keywords:** distributed systems, execution-driven simulation, parallel tracing, shared-memory multiprocessors

### 3 [Parallel simulation of chip-multiprocessor architectures](#)



Matthew Chidester, Alan George

 July 2002 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 12 Issue 3


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IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

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